SPECIFICATIONS FOR OLED MODULE

MODEL NO.
BL25664BWRNHn$
VER01

OR MESSRS:

_____

ON DATE OF:

_____

APPROVED BY:

_____

BOLYMIN, INC.
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History of Version

Version	Contents	Date	Note
01	NEW VERSION	2008/11/12	SPEC.

C O N T E N T S

1. Numbering System

	B	L	25664	B	W	R	N	-	H	n$
	0	1	2	3	4	5	6	7	8	9

0	Brand	Bolymin	
1	Module Type	C= character type G= graphic type P= TAB/TCP type	O= COG type F= COF type L=PLED/OLED
2	Format	2002=20 characters, 2 lines 12232= 122 x 32 dots	
3	Version No.	A type	
4	LCD Color	G=STN/gray Y=STN/yellow-green PLED/yellow-green C=color STN,OLED/RGB W= OLED white	B=STN/blue,OLED/blue F=FSTN T=TN D=OLED/blue+yellow A=OLED/blue+yellow+green
5	LCD Type	R=positive/reflective P=positive/transflective	M=positive/transmissive N=negative/transmissive
6	Backlight type/color	L=LED array/ yellow-green H=LED edge/white R=LED array/red G=LED edge/yellow-green F=RGB array I=RGB edge Q=LED edge/red N=No backlight	D=LED edge/blue E=EL/white B=EL/blue C=CCFL/white Y=LED Bottom/yellow O=LED array/orange K=LED edge/green A=LED edge/amber
7	CGRAM Font (applied only on character type)	J=English/Japanese Font E=English/European Font G=Chinese(simple) F=Chinese(traditional)	C=English/Cyrillic Font H=English/Hebrew Font A=English/Arabic Font
8	View Angle/ Operating Temperature	B=Bottom/Normal Temperature H=Bottom/Wide Temperature U=Bottom/Ultra wide Temperature	T=Top/Normal Temperature W=Top/Wide Temperature C=9H/Normal Temperature E=Top/ultra wide temperature
9	Special Code	3=3 volt logic power supply n=negative voltage for LCD c=cable/connector xxx=to be assigned on datasheet	t=temperature compensation for LCD p=touch panel $=RoHS

2. General Specification

(1) Mechanical Dimension

Item	Standard Value	Unit
Number of dots	256x64	dots
Module dimension (L*W*H)	87.4*28.5*2.01(MAX)	mm
Active area	79.084*19.756	mm
Dot size	0.289(W)X0.289(H)	mm
Dot pitch	0.309(W)X0.309 (H)	mm
Color	White	

(2) Controller IC: SSD1322 Controller

(3) Temperature Range

Operating	-40 ~ +70℃
Storage	-40 ~ +85℃

3. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-40	—	+70	℃
Storage Temperature	TST	-40	—	+85	℃
Humidity		—	—	85	%
Supply Voltage For Logic	VDD	2.4	—	3.5	V
Supply Voltage For Panel	Vcc	10	—	20	V
Operating lifetime			19000(*)		Hrs

*:60cd/m^2 light on

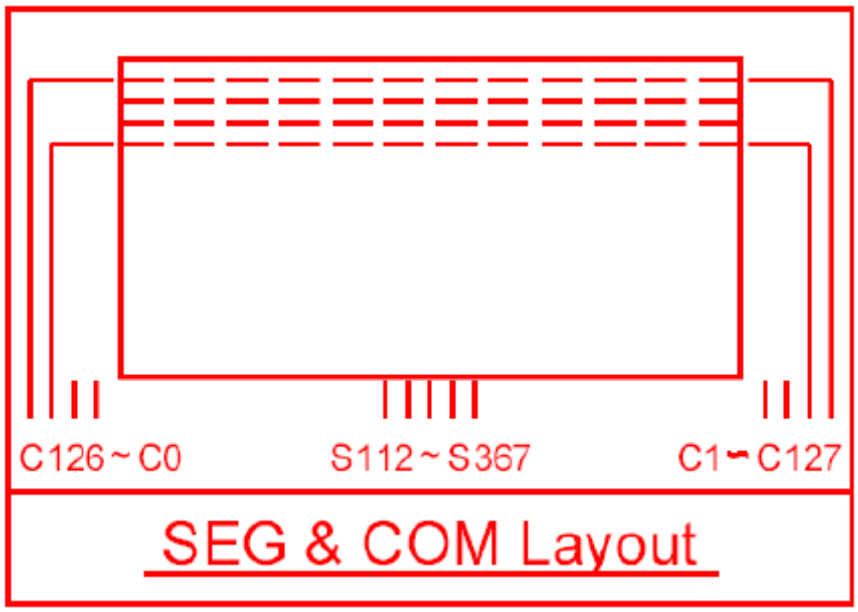
4. Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage For Logic	V_{DD}-V_{SS}	—	2.4	3.3	3.5	V
Supply Voltage For Panel	Vcc-V_{SS}	—	13.5	14	14.5	V
Input High Vol	V_{IH}	—	0.8V_{DD}	—	V_{DD}	V
Input Low Vol	V_{IL}	—	0	—	0.2V_{DD}	V
Output High Vol	V_{OH}	—	0.9V_{DD}	—	V_{DD}	V
Output Low Vol.	V_{OL}	—	0	—	0.1V_{DD}	V
Supply Current For Logic (with built-in positive voltage)	I_{DD}	—	—	270	—	mA

5. Optical Characteristics

Item	Min.	Typ.	Max.	Unit
View Angle	160	—	—	deg
Dark Room contrast	2000:1	—	—	—
Response Time	—	10	—	us

6. Panel Layout Diagram



7. Interface Pin Function

Pin No.	Symbol	Level	Description
1	Vss	0V	Ground
2	Vdd	3.3V	Supply voltage for logic
3	CS	H/L	Chip select pin
4	/RES	H/L	Hardware Reset pin
5	D/C	H/L	H: Data; L: Command.
6	WR	H/L	write signal pin
7	RD	H/L	Read signal pin
8	DB0	H/L	Data bus line
9	DB1	H/L	Data bus line
10	DB2	H/L	Data bus line
11	DB3	H/L	Data bus line
12	DB4	H/L	Data bus line
13	DB5	H/L	Data bus line
14	DB6	H/L	Data bus line
15	DB7	H/L	Data bus line
16	DISPOFF/ VCC	— H/L	DISPOFF: Active L VCC: supply voltage for panel(optional)

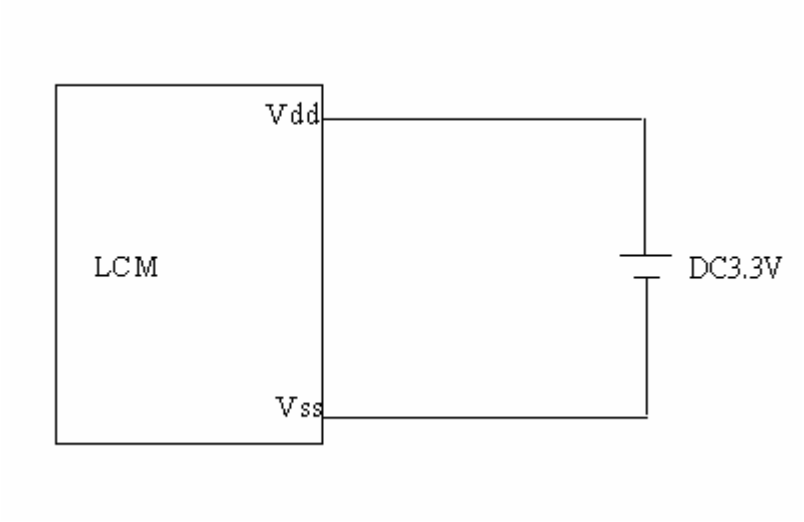
Default: Parallel 8-Bit 8080 Interface
68j : Parallel 8-Bit 6800 Interface Special Code
20i : SPI Interface Special Code

MCU interface assignment under different bus interface mode

Pin Name / Bus Interface	Data/Command Interface								Control Signal				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
3-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	Tie LOW	RES#
4-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	D/C#	RES#

8. Power Supply For OLED Module

＊ OLED Module operating on "DC 3.3V " input with built-in positive voltage



9. Timing Characteristics

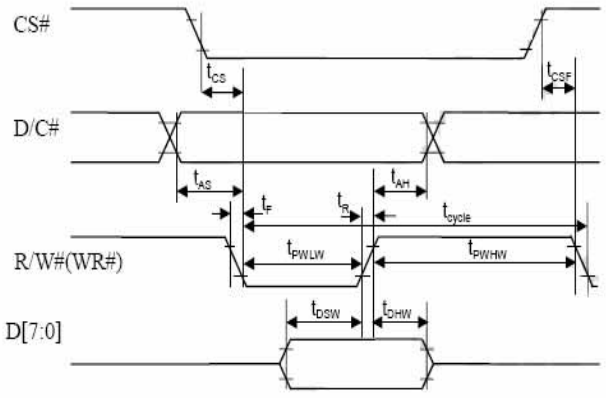
9-1.8080 MPU Interface

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

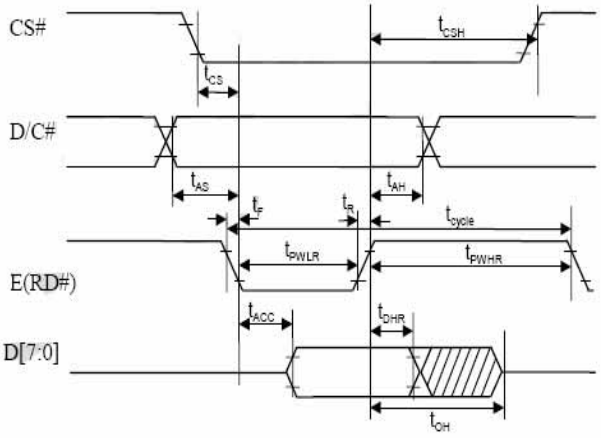
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series MCU parallel interface characteristics

Write cycle



Read cycle

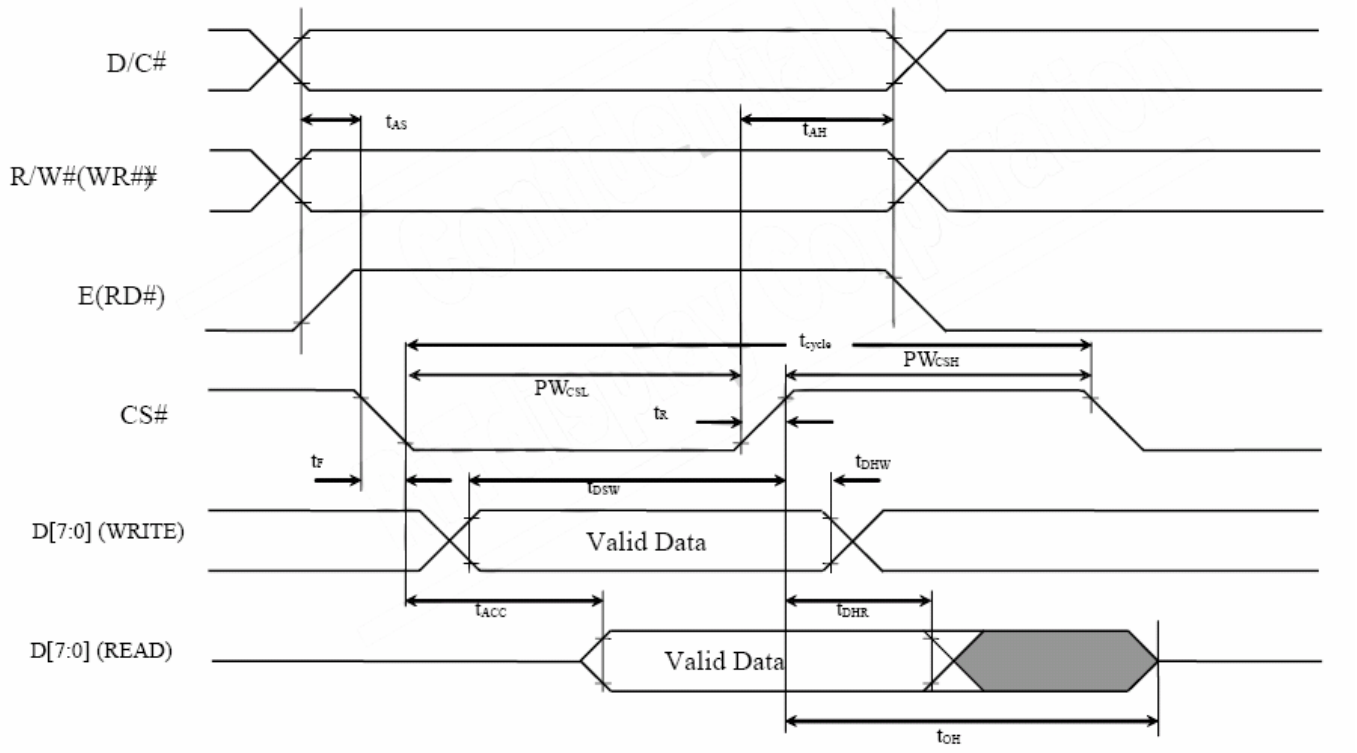


9-2.6800 MPU Interface

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

6800-series MCU parallel interface characteristics

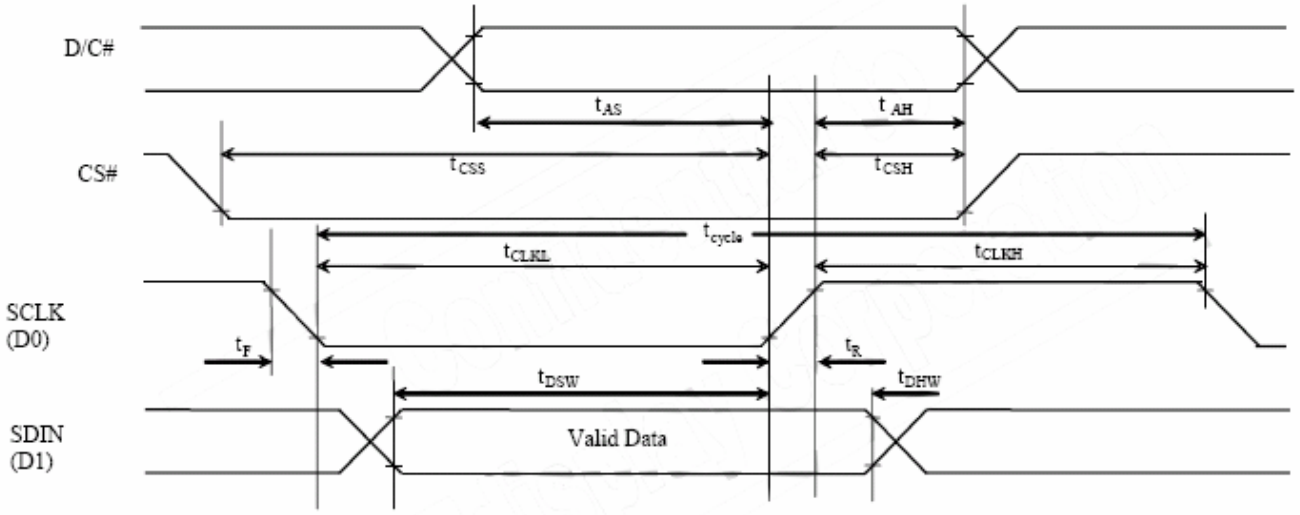


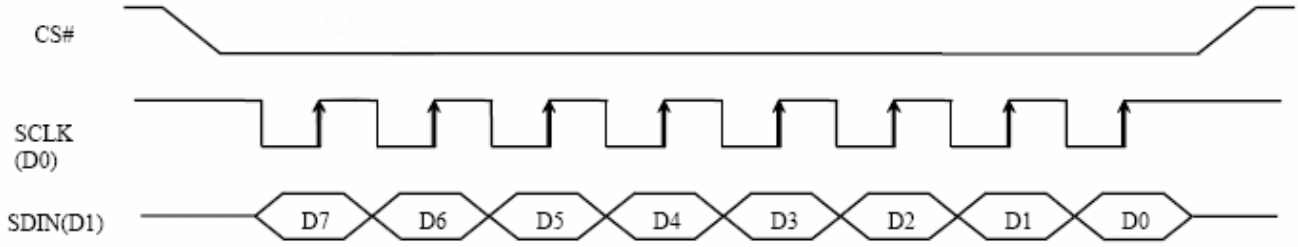
9-3.Serial Interface(4-wire SPI)

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Serial interface characteristics (4-wire SPI)



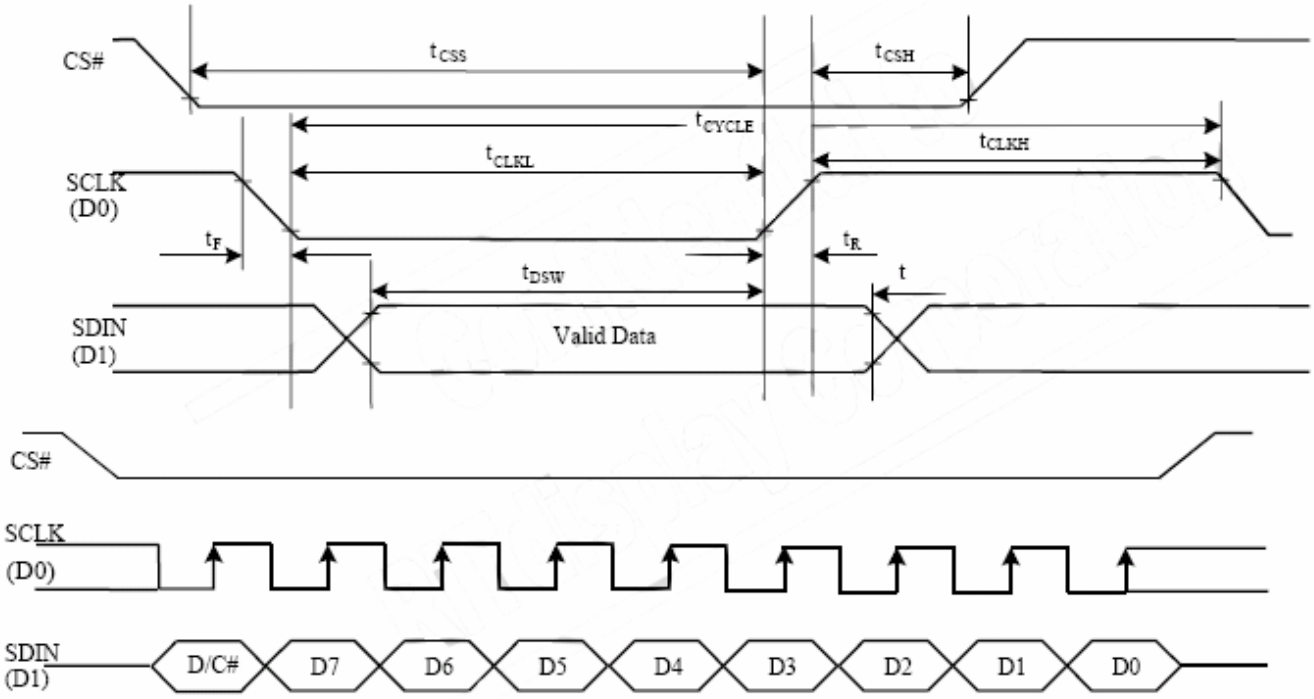


9-4.Serial Interface (3-wire SPI)

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Serial interface characteristics (3-wire SPI)

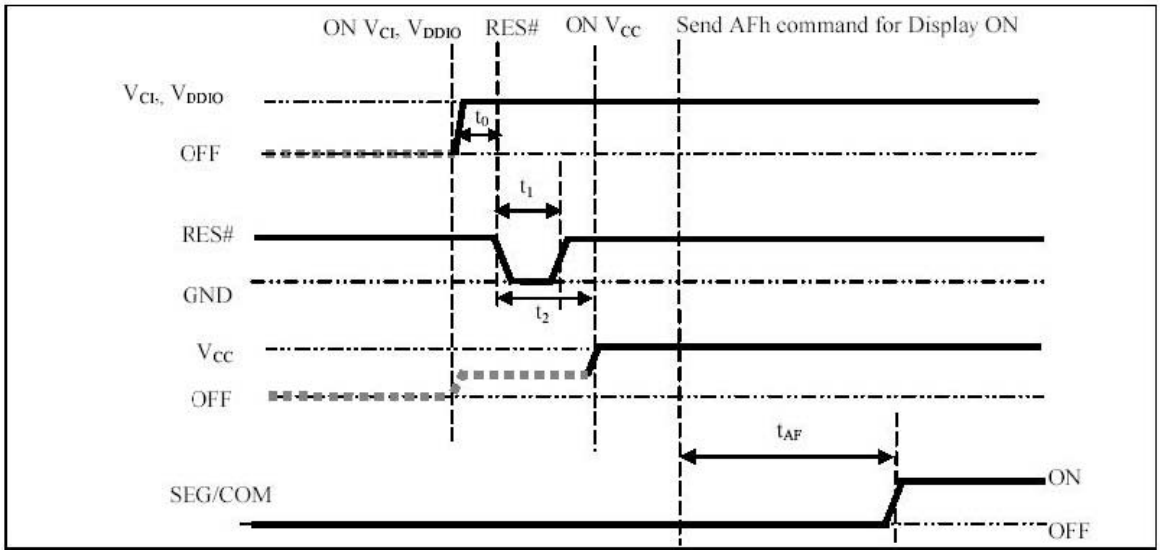


10. Power ON / OFF Sequence & Application Circuit

10.1 POWER ON / OFF SEQUENCE

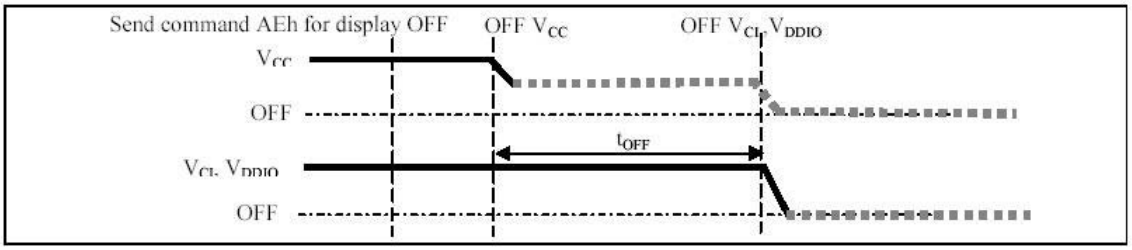
Power ON sequence:

1. Power ON VCI, VDDIO.
2. After VCI, VDDIO become stable, set wait time at least 1ms (t0) for internal VDD become stable. Then set RES# pin LOW (logic low) for at least 100us (t1) (4) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t2). Then Power ON VCC.(1)
4. After VCC become stable, send command AFh for display ON. SEG/COM will be ON after 200ms (tAF).



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF VCC.(1), (2)
3. Wait for tOFF. Power OFF VCI, VDDIO. (where Minimum tOFF=80ms (3), Typical tOFF=100ms)



Note:

(1) Since an ESD protection circuit is connected between VCI, VDDIO and VCC, VCC becomes lower than VCI whenever VCI,VDDIO is ON and VCC is OFF as shown in the dotted line of VCC.
(2) VCC should be kept float (disable) when it is OFF.
(3) VCI, VDDIO should not be Power OFF before VCC Power OFF.
(4) The register values are reset after t1.
(5) Power pins (VCI, VCC) can never be pulled to ground under any circumstance.

11. Display Control Instruction

(D/C#=0, R/W#(WR#) = 0, E(RD#)=1) unless specific setting is stated)

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	00	0	0	0	0	0	0	0	0	Enable Gray Scale table	This command is sent to enable the Gray Scale table setting (command B8h)
0 1 1	15 A[6:0] B[6:0]	0 * *	0 A_6 B_6	0 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Set Column start and end address A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=119] Range from 0 to 119
0	5C	0	1	0	1	1	1	0	0	Write RAM Command	Enable MCU to write Data into RAM
0	5D	0	1	0	1	1	1	0	1	Read RAM Command	Enable MCU to read Data from RAM
0 1 1	75 A[6:0] B[6:0]	0 * *	1 A_6 B_6	1 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Row Address	Set Row start and end address A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=127] Range from 0 to 127
0 1 1	A0 A[7:0] B[4]	1 0 *	0 0 *	1 A_5 0	0 A_4 B_4	0 0 0	0 A_2 0	0 A_1 0	0 A_0 1	Set Re-map and Dual COM Line mode	A[0]=0b, Horizontal address increment [reset] A[0]=1b, Vertical address increment A[1]=0b, Disable Column Address Re-map [reset] A[1]=1b, Enable Column Address Re-map A[2]=0b, Disable Nibble Re-map [reset] A[2]=1b, Enable Nibble Re-map A[4]=0b, Scan from COM0 to COM[N –1] [reset] A[4]=1b, Scan from COM[N-1] to COM0, where N is the Multiplex ratio A[5]=0b, Disable COM Split Odd Even [reset] A[5]=1b, Enable COM Split Odd Even B[4], Enable / disable Dual COM Line mode 00b, Disable Dual COM mode [reset] 01b, Enable Dual COM mode (MUX ≤ 63) Note (1) COM Split Odd Even mode must be disabled (A[5]=0b) when enabling the Dual COM mode (B[4]=1b) Details refer to Section 10.1.6
0 1	A1 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	Set display RAM display start line register from 0-127 Display start line register is reset to 00h after RESET

<table>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D2</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0
1</td><td>A2
A[6:0]</td><td>1
*</td><td>0
A_6</td><td>1
A_5</td><td>0
A_4</td><td>0
A_3</td><td>0
A_2</td><td>1
A_1</td><td>0
A_0</td><td>Set Display Offset</td><td>Set vertical scroll by COM from 0-127
The value is reset to 00H after RESET</td></tr>
<tr><td>0</td><td>A4~A7</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>X_2</td><td>X_1</td><td>X_0</td><td>Set Display Mode</td><td>A4h = Entire Display OFF, all pixels turns OFF in GS level 0

A5h = Entire Display ON, all pixels turns ON in GS level 15

A6h = Normal Display [reset]

A7h = Inverse Display (GS0 → GS15, GS1 → GS14, GS2 → GS13, …)</td></tr>
<tr><td>0
1
1</td><td>A8
A[6:0]
B[6:0]</td><td>1
0
0</td><td>0
A_6
B_6</td><td>1
A_5
B_5</td><td>0
A_4
B_4</td><td>1
A_3
B_3</td><td>0
A_2
B_2</td><td>0
A_1
B_1</td><td>0
A_0
B_0</td><td>Enable Partial Display</td><td>This command turns ON partial mode. The partial mode display area is defined by the following two parameters,

A[6:0]: Address of start row in the display area
B[6:0]: Address of end row in the display area,
where B[6:0] must be ≥ A[6:0]</td></tr>
<tr><td>0</td><td>A9</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Exit Partial Display</td><td>This command is sent to exit the Partial Display mode</td></tr>
<tr><td>0
1</td><td>AB
A[0]</td><td>1
0</td><td>0
0</td><td>1
0</td><td>0
0</td><td>1
0</td><td>0
0</td><td>1
0</td><td>1
A_0</td><td>Function Selection</td><td>A[0]=0b, Select external V_{DD}
A[0]=1b, Enable internal V_{DD} regulator [reset]</td></tr>
<tr><td>0</td><td>AE~AF</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>X_0</td><td>Set Sleep mode ON/OFF</td><td>AEh = Sleep mode ON (Display OFF)
AFh = Sleep mode OFF (Display ON)</td></tr>
<tr><td>0
1</td><td>B1
A[7:0]</td><td>1
A_7</td><td>0
A_6</td><td>1
A_5</td><td>1
A_4</td><td>0
A_3</td><td>0
A_2</td><td>0
A_1</td><td>1
A_0</td><td>Set Phase Length</td><td>A[3:0] Phase 1 period (reset phase length) of 5~31 DCLK(s) clocks as follow:

<table><tr><th>A[3:0]</th><th>Phase 1 period</th></tr><tr><td>0000</td><td>invalid</td></tr><tr><td>0001</td><td>invalid</td></tr><tr><td>0010</td><td>5 DCLKs</td></tr><tr><td>0011</td><td>7 DCLKs</td></tr><tr><td>0100</td><td>9 DCLKs [reset]</td></tr><tr><td>:</td><td>:</td></tr><tr><td>1111</td><td>31 DCLKs</td></tr></table>
A[7:4] Phase 2 period (first pre-charge phase length) of 3~15 DCLK(s) clocks as follow:

<table><tr><th>A[7:4]</th><th>Phase 2 period</th></tr><tr><td>0000</td><td>invalid</td></tr><tr><td>0001</td><td>invalid</td></tr><tr><td>0010</td><td>invalid</td></tr><tr><td>0011</td><td>3 DCLKs</td></tr><tr><td>:</td><td>:</td></tr><tr><td>0111</td><td>7 DCLKs [reset]</td></tr><tr><td>:</td><td>:</td></tr><tr><td>1111</td><td>15 DCLKs</td></tr></table></td></tr>
</table>

<table>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D2</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0
1</td><td>B3
A[7:0]</td><td>1
A_7</td><td>0
A_6</td><td>1
A_5</td><td>1
A_4</td><td>0
A_3</td><td>0
A_2</td><td>1
A_1</td><td>1
A_0</td><td>Set Front Clock Divider / Oscillator Frequency</td><td>A[3:0] [reset=0], divide by DIVSET where
<table><tr><th>A[3:0]</th><th>DIVSET</th></tr><tr><td>0000</td><td>divide by 1</td></tr><tr><td>0001</td><td>divide by 2</td></tr><tr><td>0010</td><td>divide by 4</td></tr><tr><td>0011</td><td>divide by 8</td></tr><tr><td>0100</td><td>divide by 16</td></tr><tr><td>0101</td><td>divide by 32</td></tr><tr><td>0110</td><td>divide by 64</td></tr><tr><td>0111</td><td>divide by 128</td></tr><tr><td>1000</td><td>divide by 256</td></tr><tr><td>1001</td><td>divide by 512</td></tr><tr><td>1010</td><td>divide by 1024</td></tr><tr><td>>=1011</td><td>invalid</td></tr></table>
A[7:4] Oscillator frequency, frequency increases as level increases [reset=1100b]</td></tr>
<tr><td>0
1
1</td><td>B4
A[1:0]
B[7:3]</td><td>1
1
B_7</td><td>0
0
B_6</td><td>1
1
B_5</td><td>1
0
B_4</td><td>0
0
B_3</td><td>1
0
1</td><td>0
A_1
0</td><td>0
A_0
1</td><td>Display Enhancement A</td><td>A[1:0] = 00b: Enable external VSL
A[1:0] = 10b: Internal VSL [reset]

B[7:3] = 11111b: Enhanced low GS display quality
B[7:3] = 10110b: Normal [reset]</td></tr>
<tr><td>0
1</td><td>B5
A[3:0]</td><td>1
*</td><td>0
*</td><td>1
*</td><td>1
*</td><td>0
A_3</td><td>1
A_2</td><td>0
A_1</td><td>1
A_0</td><td>Set GPIO</td><td>A[1:0] GPIO0: 00 pin HiZ, Input disabled
01 pin HiZ, Input enabled
10 pin output LOW [reset]
11 pin output HIGH

A[3:2] GPIO1: 00 pin HiZ, Input disabled
01 pin HiZ, Input enabled
10 pin output LOW [reset]
11 pin output HIGH</td></tr>
<tr><td>0
1</td><td>B6
A[3:0]</td><td>1
*</td><td>0
*</td><td>1
*</td><td>1
*</td><td>0
A_3</td><td>1
A_2</td><td>1
A_1</td><td>0
A_0</td><td>Set Second Precharge Period</td><td>A[3:0] Second Pre-charge period
0000b 0 dclk
0001b 1 dclk
……
1000b 8 dclks [reset]
……
1111b 15 dclks</td></tr>
<tr><td>0
1
1
1
1
1
1
1</td><td>B8
A1[7:0]
A2[7:0]
.
.
.
A14[7:0]
A15[7:0]</td><td>1
$A1_7$
$A2_7$
.
.
.
$A14_7$
$A15_7$</td><td>0
$A1_6$
$A2_6$
.
.
.
$A14_6$
$A15_6$</td><td>1
$A1_5$
$A2_5$
.
.
.
$A14_5$
$A15_5$</td><td>1
$A1_4$
$A2_4$
.
.
.
$A14_4$
$A15_4$</td><td>1
$A1_3$
$A2_3$
.
.
.
$A14_3$
$A15_3$</td><td>0
$A1_2$
$A2_2$
.
.
.
$A14_2$
$A15_2$</td><td>0
$A1_1$
$A2_1$
.
.
.
$A14_1$
$A15_1$</td><td>0
$A1_0$
$A2_0$
.
.
.
$A14_0$
$A15_0$</td><td>Set Gray Scale Table</td><td>The next 15 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d)

A1[7:0]: Gamma Setting for GS1,
A2[7:0]: Gamma Setting for GS2,
:
A14[7:0]: Gamma Setting for GS14,
A15[7:0]: Gamma Setting for GS15</td></tr>
</table>

<table>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D2</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>Note
(1) 0 ≤ Setting of GS1 < Setting of GS2 < Setting of GS3..... < Setting of GS14 < Setting of GS15

Refer to Section 8.8 for details

(2) The setting must be followed by the Enable Gray Scale Table command (00h)</td></tr>
<tr><td>0</td><td>B9</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Select Default Linear Gray Scale table</td><td>The default Linear Gray Scale table is set in unit of DCLK's as follow

GS0 level pulse width = 0;
GS1 level pulse width = 0;
GS2 level pulse width = 8;
GS3 level pulse width = 16;
:
:
GS14 level pulse width = 104;
GS15 level pulse width = 112

Refer to Section 8.8 for details</td></tr>
<tr><td>0
1</td><td>BB
A[4:0]</td><td>1
*</td><td>0
*</td><td>1
*</td><td>1
A_4</td><td>1
A_3</td><td>0
A_2</td><td>1
A_1</td><td>1
A_0</td><td>Set Pre-charge voltage</td><td>Set pre-charge voltage level [reset = 17h]
<table><tr><th>A[5:1]</th><th>Hex code</th><th>pre-charge voltage</th></tr><tr><td>00000</td><td>00h</td><td>0.20 x V_{CC}</td></tr><tr><td>:</td><td>:</td><td>:</td></tr><tr><td>11111</td><td>3Eh</td><td>0.60 x V_{CC}</td></tr></table></td></tr>
<tr><td>0
1</td><td>BE
A[3:0]</td><td>1
*</td><td>0
*</td><td>1
*</td><td>1
*</td><td>1
A_3</td><td>1
A_2</td><td>1
A_1</td><td>0
A_0</td><td>Set V_{COMH}</td><td>Set COM deselect voltage level [reset = 04h]
A[3:0] =
<table><tr><th>A[2:0]</th><th>Hex code</th><th>V_{COMH}</th></tr><tr><td>0000</td><td>00h</td><td>0.72 x V_{CC}</td></tr><tr><td>:</td><td>:</td><td>:</td></tr><tr><td>0100</td><td>04h</td><td>0.80 x V_{CC}</td></tr><tr><td>:</td><td>:</td><td>:</td></tr><tr><td>0111</td><td>07h</td><td>0.86 x V_{CC}</td></tr></table></td></tr>
<tr><td>0
1</td><td>C1
A[7:0]</td><td>1
A_7</td><td>1
A_6</td><td>0
A_5</td><td>0
A_4</td><td>0
A_3</td><td>0
A_2</td><td>0
A_1</td><td>1
A_0</td><td>Set Contrast Current</td><td>A[7:0]: Contrast current value, range:00h~FFh,
i.e. 256 steps for I_{SEG} current [reset = 7Fh]</td></tr>
<tr><td>0
1</td><td>C7
A[3:0]</td><td>1
*</td><td>1
*</td><td>0
*</td><td>0
*</td><td>0
A_3</td><td>1
A_2</td><td>1
A_1</td><td>1
A_0</td><td>Master Contrast Current Control</td><td>A[3:0] =
0000b, reduce output currents for all colors to 1/16
0001b, reduce output currents for all colors to 2/16
:
1110b, reduce output currents for all colors to 15/16
1111b, no change [reset]</td></tr>
<tr><td>0
1</td><td>CA
A[6:0]</td><td>1
*</td><td>1
A_6</td><td>0
A_5</td><td>0
A_4</td><td>1
A_3</td><td>0
A_2</td><td>1
A_1</td><td>0
A_0</td><td>Set MUX Ratio</td><td>A[6:0]: Set MUX ratio from 16MUX ~ 128MUX

A[6:0] = 15d represents 16MUX
:
A[6:0] = 127d represents 128MUX [reset]</td></tr>
</table>

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	D1	1	1	0	1	0	0	0	1		
1	A[5:4]	1	0	A_5	A_4	0	0	1	0	Display Enhancement B	A[5:4] = 00b: Reserved A[5:4] = 10b: Normal [reset]
1	20	0	0	1	0	0	0	0	0		
0	FD	1	1	1	1	1	1	0	1	Set Command Lock	A[2]: MCU protection status [reset = 12h] A[2] = 0b, Unlock OLED driver IC MCU interface from entering command [reset] A[2] = 1b, Lock OLED driver IC MCU interface from entering command Note (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command
1	A[2]	0	0	0	1	0	A_2	1	0		

Note
(1) "*" stands for "Don't care".

12. Reliability

■Content of Reliability Test

NO.	Items.	Specification	Applicable Standard
1	High temp. (Non-operation)	85°C, 240hrs	——
2	High temp. (Operation)	70°C, 120hrs	——
3	Low temp. (Operation)	-40°C, 120hrs	——
4	High temp. / High. humidity (Operation)	65°C, 90%RH, 120hrs	——
5	Thermal shock(Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles.	——
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	——
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and faces Cycles: 1	——
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	——

13. Appendix (Drawing)