

NC7S04 TinyLogic® HS Inverter

General Description

The NC7S04 is a single high performance CMOS Inverter. Advanced Silicon Gate CMOS fabrication assures high speed and low power circuit operation over a broad V_{CC} range. ESD protection diodes inherently guard both input and output with respect to the V_{CC} and GND rails. Three stages of gain between input and output assures high noise immunity and reduced sensitivity to input edge rate.

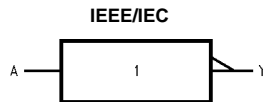
Features

- Space saving SOT23 or SC70 5-lead package
- Ultra small MicroPak™ leadless package
- High Speed: $t_{PD} = 3$ ns typ
- Low Quiescent Power: $I_{CC} < 1 \mu A$
- Balanced Output Drive: 2 mA I_{OL} , -2 mA I_{OH}
- Broad V_{CC} Operating Range: 2V – 6V
- Balanced Propagation Delays
- Specified for 3V operation

Ordering Code:

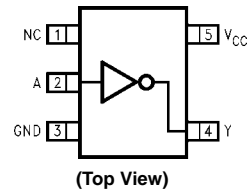
| Order Number | Package Number | Product Code Top Mark | Package Description | Supplied As |
|--------------|----------------|-----------------------|---------------------------------------|---------------------------|
| NC7S04M5X | MA05B | 7S04 | 5-Lead SOT23, JEDEC MO-178, 1.6mm | 3k Units on Tape and Reel |
| NC7S04P5X | MAA05A | S04 | 5-Lead SC70, EIAJ SC-88a, 1.25mm Wide | 3k Units on Tape and Reel |
| NC7S04L6X | MAC06A | AA | 6-Lead MicroPak, 1.0mm Wide | 5k Units on Tape and Reel |

Logic Symbol



Connection Diagrams

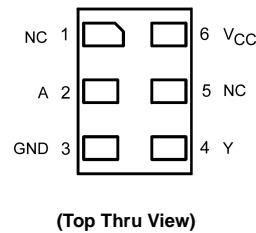
Pin Assignments for SC70 and SOT23



Pin Descriptions

| Pin Names | Description |
|-----------|-------------|
| A | Input |
| Y | Output |
| NC | No Connect |

Pad Assignments for MicroPak



Function Table

$$Y = \bar{A}$$

| Input | Output |
|-------|--------|
| A | Y |
| L | H |
| H | L |

H = HIGH Logic Level
L = LOW Logic Level

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MicroPak™ is a trademark of Fairchild Semiconductor Corporation.

| Absolute Maximum Ratings (Note 1) | | Recommended Operating Conditions (Note 2) | |
|--|--------------------------|---|----------------|
| Supply Voltage (V_{CC}) | -0.5V to +7.0V | Supply Voltage (V_{CC}) | 2.0V to 6.0V |
| DC Input Diode Current (I_{IK}) | | Input Voltage (V_{IN}) | 0V to V_{CC} |
| @ $V_{IN} \leq -0.5V$ | -20 mA | Output Voltage (V_{OUT}) | 0V to V_{CC} |
| @ $V_{IN} \geq V_{CC} + 0.5V$ | +20 mA | Operating Temperature (T_A) | -40°C to +85°C |
| DC Input Voltage (V_{IN}) | -0.5V to $V_{CC} + 0.5V$ | Input Rise and Fall Time (t_r, t_f) | |
| DC Output Diode Current (I_{OK}) | | $V_{CC} @ 2.0V$ | 0 to 1000 ns |
| @ $V_{OUT} \leq -0.5V$ | -20 mA | $V_{CC} @ 3.0V$ | 0 to 750 ns |
| @ $V_{OUT} \geq V_{CC} + 0.5V$ | +20 mA | $V_{CC} @ 4.5V$ | 0 to 500 ns |
| DC Output Voltage (V_{OUT}) | -0.5V to $V_{CC} + 0.5V$ | $V_{CC} @ 6.0V$ | 0 to 400 ns |
| DC Output Source or Sink Current (I_{OUT}) | ± 12.5 mA | Thermal Resistance (θ_{JA}) | |
| DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) | ± 25 mA | SOT23-5 | 300°C/W |
| Storage Temperature (T_{STG}) | -65°C to +150°C | SC70-5 | 425°C/W |
| Junction Temperature (T_J) | 150°C | Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, with-out exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of circuits outside the databook specifications. | |
| Lead Temperature (T_L) (Soldering, 10 seconds) | 260°C | Note 2: Unused inputs must be held HIGH or LOW. They may not float. | |
| Power Dissipation (P_D) @ +85°C | | | |
| SOT23-5 | 200 mW | | |
| SC70-5 | 150 mW | | |

DC Electrical Characteristics

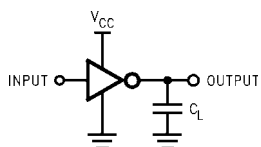
| Symbol | Parameter | V_{CC} (V) | $T_A = +25^\circ C$ | | | $T_A = -40^\circ C$ to $+85^\circ C$ | | Units | Conditions | |
|----------|---------------------------|--------------|---------------------|-----------|--------------|--------------------------------------|--------------|------------------------|---|---|
| | | | Min | Typ | Max | Min | Max | | | |
| V_{IH} | HIGH Level Input Voltage | 2.0 | 1.50 | | | 1.50 | | V | | |
| | | 3.0 - 6.0 | 0.7 V_{CC} | | | 0.7 V_{CC} | | | | |
| V_{IL} | LOW Level Input Voltage | 2.0 | | | 0.50 | | 0.50 | V | | |
| | | 3.0 - 6.0 | | | 0.3 V_{CC} | | 0.3 V_{CC} | | | |
| V_{OH} | HIGH Level Output Voltage | 2.0 | 1.90 | 2.0 | | 1.90 | | V | $I_{OH} = -20 \mu A$ $V_{IN} = V_{IL}$ | |
| | | 3.0 | 2.90 | 3.0 | | 2.90 | | | | |
| | | 4.5 | 4.40 | 4.5 | | 4.40 | | | | |
| | | 6.0 | 5.90 | 6.0 | | 5.90 | | | | |
| | | | 3.0 | 2.68 | 2.85 | | 2.63 | | V | $V_{IN} = V_{IL}$ $I_{OH} = -1.3$ mA $I_{OH} = -2.0$ mA $I_{OH} = -2.6$ mA |
| | | | 4.5 | 4.18 | 4.35 | | 4.13 | | | |
| | | | 6.0 | 5.68 | 5.85 | | 5.63 | | | |
| | | | | | | | | | | |
| V_{OL} | LOW Level Output Voltage | 2.0 | | 0.0 | 0.10 | | 0.10 | V | $I_{OL} = 20 \mu A$ $V_{IN} = V_{IH}$ | |
| | | 3.0 | | 0.0 | 0.10 | | 0.10 | | | |
| | | 4.5 | | 0.0 | 0.10 | | 0.10 | | | |
| | | 6.0 | | 0.0 | 0.10 | | 0.10 | | | |
| | | | 3.0 | | 0.1 | 0.26 | | 0.33 | V | $V_{IN} = V_{IH}$ $I_{OL} = 1.3$ mA $I_{OL} = 2.0$ mA $I_{OL} = 2.6$ mA |
| | | | 4.5 | | 0.1 | 0.26 | | 0.33 | | |
| | | | 6.0 | | 0.1 | 0.26 | | 0.33 | | |
| | | | | | | | | | | |
| I_{IN} | Input Leakage Current | 6.0 | | ± 0.1 | | ± 1.0 | μA | $V_{IN} = V_{CC}, GND$ | | |
| I_{CC} | Quiescent Supply Current | 6.0 | | 1.0 | | 10.0 | μA | $V_{IN} = V_{CC}, GND$ | | |

AC Electrical Characteristics

| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | | T _A = -40°C to +85°C | | Units | Conditions | Figure Number |
|------------------|-------------------------------|------------------------|------------------------|-------|------|---------------------------------|-----|-------|------------------------|---------------|
| | | | Min | Typ | Max | Min | Max | | | |
| t _{PLH} | Propagation Delay | 5.0 | | 3.0 | 15.0 | | | ns | C _L = 15 pF | Figures 1, 3 |
| t _{PHL} | | 2.0 | 18.0 | 100.0 | | 125.0 | | ns | C _L = 50 pF | |
| | | 3.0 | 10.0 | 27.0 | | 35.0 | | | | |
| | | 4.5 | 7.0 | 20.0 | | 25.0 | | | | |
| | | 6.0 | 6.0 | 17.0 | | 21.0 | | | | |
| t _{TLH} | Output Transition Time | 5.0 | 3.0 | 10.0 | | | | ns | C _L = 15 pF | Figures 1, 3 |
| t _{THL} | | 2.0 | 25.0 | 125.0 | | 155.0 | | ns | C _L = 50 pF | |
| | | 3.0 | 16.0 | 35.0 | | 45.0 | | | | |
| | | 4.5 | 11.0 | 25.0 | | 31.0 | | | | |
| | | 6.0 | 9.0 | 21.0 | | 26.0 | | | | |
| C _{IN} | Input Capacitance | Open | 2.0 | 10.0 | | 10.0 | | pF | | |
| C _{PD} | Power Dissipation Capacitance | 5.0 | 6.0 | | | | | pF | (Note 3) | Figure 2 |

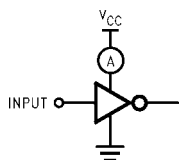
Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression:
 $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CCstatic})$.

AC Loading and Waveforms



C_L includes load and stray capacitance
 Input PRR = 1.0 MHz, t_w = 500 ns

FIGURE 1. AC Test Circuit



Input = AC Waveforms;
 PRR = Variable; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

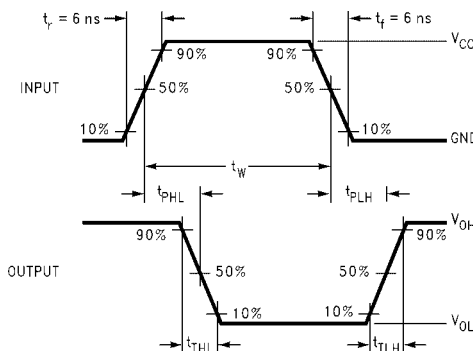


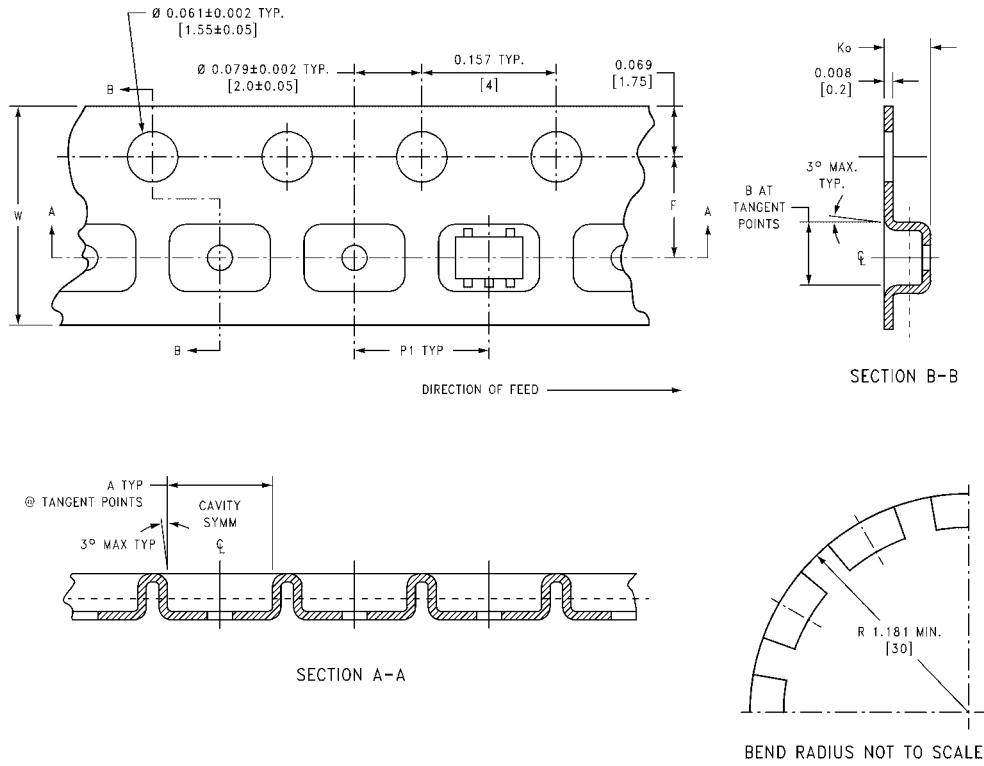
FIGURE 3. AC Waveforms

Tape and Reel Specification

TAPE FORMAT FOR SOT23, SC70

| Package Designator | Tape Section | Number Cavities | Cavity Status | Cover Tape Status |
|--------------------|--------------------|-----------------|---------------|-------------------|
| M5X, P5X | Leader (Start End) | 125 (typ) | Empty | Sealed |
| | Carrier | 3000 | Filled | Sealed |
| | Trailer (Hub End) | 75 (typ) | Empty | Sealed |

TAPE DIMENSIONS inches (millimeters)



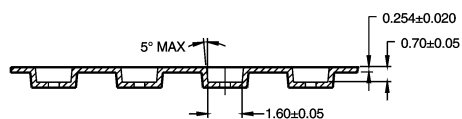
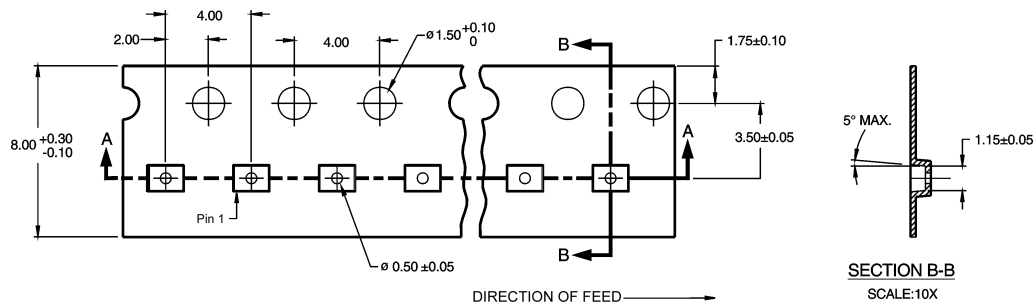
| Package | Tape Size | DIM A | DIM B | DIM F | DIM K ₀ | DIM P1 | DIM W |
|---------|-----------|-----------------|-----------------|-------------------------------|--------------------------------|--------------|----------------------------|
| SC70-5 | 8 mm | 0.093 (2.35) | 0.096 (2.45) | 0.138 ± 0.004 (3.5 ± 0.10) | 0.053 ± 0.004 (1.35 ± 0.10) | 0.157 (4) | 0.315 ± 0.004 (8 ± 0.1) |
| SOT23-5 | 8 mm | 0.130 (3.3) | 0.130 (3.3) | 0.138 ± 0.002 (3.5 ± 0.05) | 0.055 ± 0.004 (1.4 ± 0.11) | 0.157 (4) | 0.315 ± 0.012 (8 ± 0.3) |

Tape and Reel Specification (Continued)

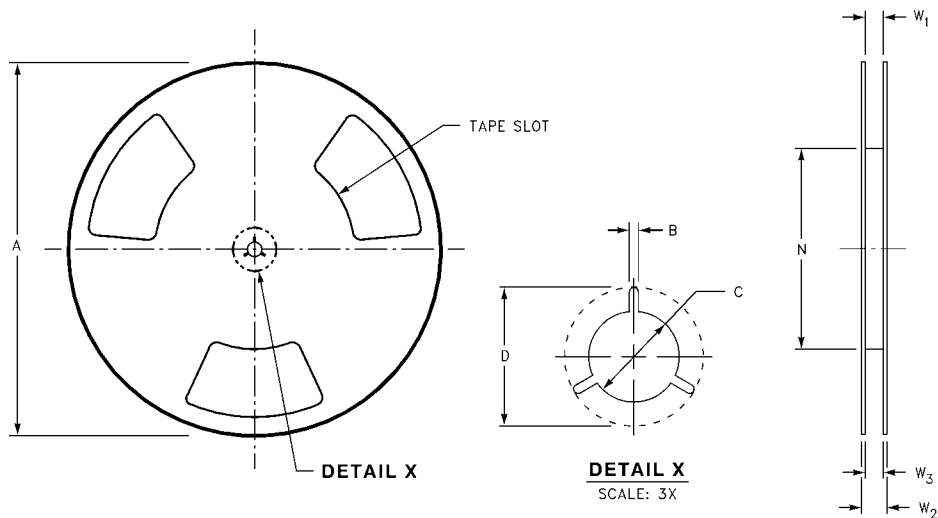
TAPE FORMAT FOR MicroPak

| Package Designator | Tape Section | Number Cavities | Cavity Status | Cover Tape Status |
|--------------------|--------------------|-----------------|---------------|-------------------|
| L6X | Leader (Start End) | 125 (typ) | Empty | Sealed |
| | Carrier | 5000 | Filled | Sealed |
| | Trailer (Hub End) | 75 (typ) | Empty | Sealed |

TAPE DIMENSIONS inches (millimeters)



REEL DIMENSIONS inches (millimeters)

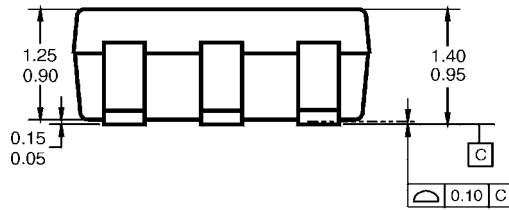


| Tape Size | A | B | C | D | N | W1 | W2 | W3 |
|-----------|----------------|-----------------|------------------|------------------|------------------|---|------------------|--|
| 8 mm | 7.0 (177.8) | 0.059 (1.50) | 0.512 (13.00) | 0.795 (20.20) | 2.165 (55.00) | 0.331 + 0.059/-0.000 (8.40 + 1.50/-0.00) | 0.567 (14.40) | W1 + 0.078/-0.039 (W1 + 2.00/-1.00) |

Physical Dimensions inches (millimeters) unless otherwise noted



LAND PATTERN RECOMMENDATION



DETAIL A

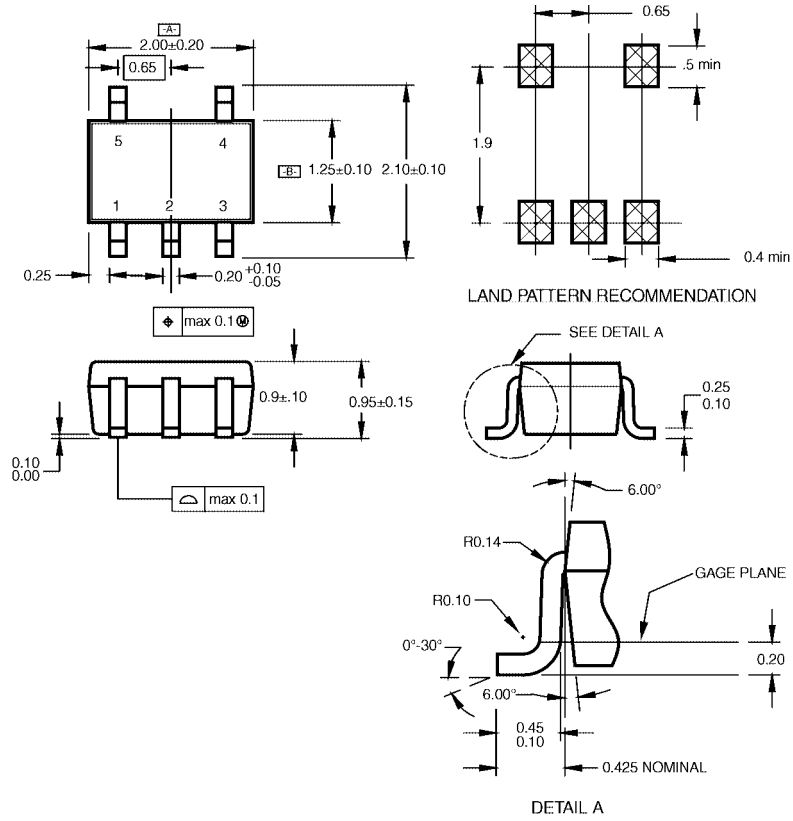
NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MO-178, ISSUE B, VARIATION AA, DATED JANUARY 1999.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.

MA05BRevC

5-Lead SOT23, JEDEC MO-178, 1.6mm
Package Number MA05B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



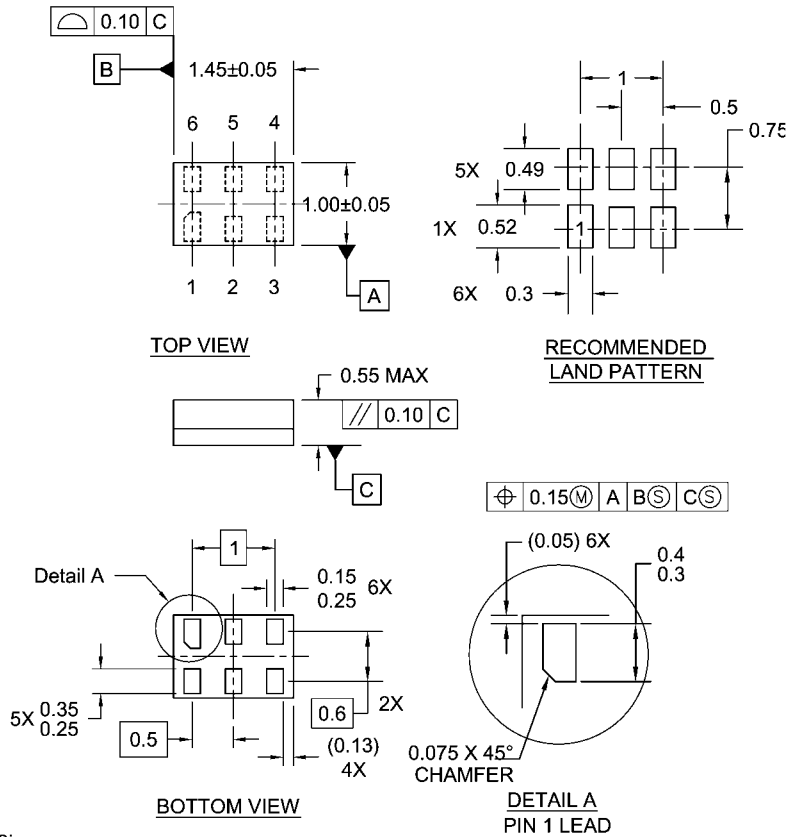
NOTES:

- A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88A.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
- C. DIMENSIONS ARE IN MILLIMETERS.

MAA05ARevC

**5-Lead SC70, EIAJ SC-88a, 1.25mm Wide
Package Number MAA05A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:

1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06ARevB

**6-Lead MicroPak, 1.0mm Wide
Package Number MAC06A**

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